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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,491	05/15/2001	Thomas Sean Houlihane	550-229	7919

23117 7590 05/20/2005

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EXAMINER
PROCTOR, JASON SCOTT

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 05/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,491	HOULIHANE ET AL.	
	Examiner	Art Unit	
	Jason Proctor	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-43* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-43* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-34 were presented for examination and rejected in the office action dated October 4, 2004. Applicants have amended claims 1, 2, 6, 12, 15, 17-19, 28, 32, and 33 and added claims 35-43. Claims 1-43 have been submitted for examination. Claims 1-43 have been rejected.

Response to Objections to the Drawings

The Examiner thanks Applicant for correcting the objections to the drawings. The Examiner thanks Applicant for clarification of the labels of the block diagram of Figure 7 and has found no new matter. The Examiner thanks Applicant for the replacement drawing sheets that comply with 37 CFR § 1.84. The objections to the drawings of the previous office action have been withdrawn.

Response to Objections to the Specification

The Examiner thanks Applicant for correcting the objections to the specification. The objections to the specification of the previous office action have been withdrawn.

Response to Objections to the Claims

The Examiner thanks Applicant for separating the elements of claims 1, 17, 19, 21, and 32 with line indentions. The objections to the claims of the previous office action have been withdrawn.

Response to Rejections under 35 U.S.C. § 112

The Examiner thanks Applicant for correcting the issues that were rejected under 35 U.S.C. § 112, second paragraph. The rejections of claims 1-17 and 28-30 have been withdrawn.

1. Regarding the rejection of claim 34 under 35 U.S.C. § 112, second paragraph, Applicant argues primarily that (emphasis added):

> Specifically, Applicants believe at least a portion of the Examiner's confusion stems from his assumption that the reduced model of claim 1 is in fact a reduced model of hardware. This is not strictly correct, and rather **the reduced model of claim 1** is **could be** [sic] a software model, **a hardware model** or a combination of software and hardware. This is clearly described in Applicants' originally filed specification at page 8, lines 6-11 describing Figure 3. Applicants believe that given the correct interpretation of the reduced model feature set out in claim 1, claim 34 makes perfect sense in that **a reduced hardware model is synthesized from a reduced model comprising a software component.**

The Examiner respectfully traverses this argument as follows.

In the previous office action, the rejection of claim 34 stated:

> It is unclear what constitutes "synthesising" a reduced hardware model from a reduced model.

Applicants' arguments support the Examiner's interpretation that the "reduced model" of claim 1 could be a hardware model and fail to clarify what is mean by "synthesizing" a reduced hardware model from a reduced (hardware) model. Applicants' clarification that a reduced hardware model is synthesized from a reduced model comprising a software component is not found in the claims. This rejection is maintained.

Response to Rejections under 35 U.S.C. § 101

The Examiner thanks Applicant for amending the language of claims 17 and 32 to place them within the four categories of statutory invention.

2. Regarding claims 18 and 33, which recite a computer program *per se*, Applicant has amended these claims to recite "A computer program on a carrier medium". The Examiner appreciates this attempt to claim the computer program as tangibly embodied as set forth by MPEP 2106, however the specification (pages 10-11 as amended) teaches the definition of "carrier medium" as both tangible and intangible:

> The computer program produced described above may take the form of a computer program stored within the computer system 200 on the hard disk drive 208, within the random access memory 204, within the read-only memory 206, or **downloaded via the network interface circuit 220**. The computer program product may also take the form of a recording medium such as a compact disk or floppy disk drive that may be used for distribution purposes.

If Applicant has provided an explicit definition of the term "carrier medium", clarification is respectfully requested. Until such clarification, the term "carrier medium" is not restricted to tangible embodiments and therefore claims 18 and 33 recite computer programs *per se* and are therefore nonstatutory. The Examiner bases this analysis on MPEP 2106:

> Since a computer program is merely a set of instructions capable of being executed by a computer, the computer program itself is not a process and Office personnel should treat a claim for a computer program, without the computer-readable medium needed to realize the computer program's functionality, as nonstatutory functional descriptive material. When a computer program is claimed in a process where the computer is executing the computer program's instructions, Office personnel should treat the claim as a process claim. See paragraph IV.B.2(b), below. When a computer program is recited in conjunction with a physical structure, such as a computer memory, Office personnel should treat the claim as a product claim. See paragraph IV.B.2(a), below.

The rejections of claims 18 and 33 under 35 U.S.C. § 101 are maintained.

3. Regarding claim 34, which recites "A reduced hardware model synthesized from said reduced model of claim 1", Applicant argues that:

> The objection to claim 34 has been previously addressed and amendments to claim 1 are believed to have obviated any further objections to claim 34.

The Examiner respectfully traverses this argument as follows:

In the previous office action, the rejection of claim 34 stated:

> Regarding claim 34, the limitations recite a data abstraction not claimed as embodied in a computer-readable media and is descriptive material *per se.* As a result, the claim is nonstatutory.

The Examiner maintains this analysis of claim 34. The "reduced hardware model" is an abstraction and not statutory. If Applicant believes the language of claim 1 or the disclosure of the application supports an interpretation of "reduced hardware model" that is restricted to a tangible apparatus, clarification is respectfully requested. This rejection is maintained.

Response to Rejections under 35 U.S.C. § 102

Regarding the rejection of claims 1-5, 12-14, 16-21, 28-30, and 32-34 under 35 U.S.C. § 102 as being anticipated by US Patent No. 5,903,475 to Gupte, Applicant argues primarily that:

> An examination of column 2, lines 7-22 of Gupte establishes that the Gupte system captures "golden" vectors that may be used to test an ASIC during stand-alone simulation and that the outputs generated by the ASIC during such simulations are comparable to the outputs generated during the system simulation itself, i.e., the golden vectors. This has nothing to do with the claimed using step, especially "without requiring a periodic sampling reference."

Applicant further argues that:

> The portion of column 6, lines 41-52 simply does not disclose or suggest that the output signals of the sub-system circuit model are tested by using a plurality of sampling rules and "without requiring a periodic sampling reference."

The Examiner respectfully traverses this argument as follows:

Gupte, column 6, lines 48-61 state:

> At step 208, the behavioral specification of the ASIC is simulated within the customer's system environment[.] Typically, the simulation is performed at the customer's site but it may also be performed at the foundry if practical[.]

> During the simulation step 208, the invention captures "golden" vectors that are used to test the ASIC during stand-alone simulation. The outputs generated by the ASIC during stand-alone simulation are then compared to the outputs generated during the system simulation. Thus, the customer's system simulation is reproduced without having to reproduce the customer's system environment which allows the operation of the ASIC to be verified during various states of synthesis as described below.

The Examiner respectfully draws Applicants' attention to the instant application, particularly Figure 4, references 28 and 34. As established in Gupte, the "golden vectors" form what Applicant refers to as "reduced model data", such as Applicants' Figure 4, reference 28. As established in Gupte, this data is used to replace the surrounding system (customer's system environment), such as Applicants' Figure 4, reference 34. The outputs generated by the ASIC during stand-alone simulation are compared to the outputs generated during the system simulation (which are the "golden vectors") (Gupte, column 6, lines 55-57), which clearly comprises "comparing output signals with predetermined characteristics indicative of correct operation".

The Examiner respectfully submits that this is entirely relevant to the claimed using step under discussion. Gupte's use of "golden vectors" is completely functionally equivalent to Applicants' claimed "reduced model", the intended use of the reduced model, and Applicants' disclosure of the reduced model as represented by Figure 4.

Regarding the phrase "without requiring a periodic sampling reference" found in amended claims 17, 19, and 32 and new claim 35, the application as originally filed provides neither adequate written disclosure nor enablement for this feature. The Examiner has entered new grounds of rejection under 35 U.S.C. § 112, first paragraph,

accordingly. Further, the disclosure of the application appears to teach, in at least one embodiment, the use of a clock during the step of replaying the model, such as:

> Page 4, lines 15-22 (emphasis added):
>
> The configuration files used in conjunction with the recorded signals could take various different forms, but are preferably files specifying whether signals are input signals, output signals or bidirectional signals. This data may then be used to control the automatic generation of the required portion of the reduced model **to replay input signals in the correct sequence and time**, or capture output signals with appropriate timing constraints and interdependencies associated therewith. This also allows timing models to be defined for association with signals thereby reducing the overall work required to produce a model.
>
> Page 4, line 30 – page 5, line 5 (emphasis added):
>
> **Some of the output signals may be strobe signals that control the sampling of other output signals and this behaviour can be modelled within the reduced model. Both the strobe output signal and the strobed output signal may have time windows associated with them.** A strobe output signal should change to its desired predetermined state (e.g. strobe signals may only be active on a rising edge and otherwise ignored) within an associated strobe output signal time window and the strobed output signals should hold their value within a strobed signal time window. The strobed signal time window may be asymmetrically disposed about is sampling point and may be surrounded by a settling window and a settled window. More than one signal may strobe a strobed signal.
>
> Page 7, lines 13-17 (emphasis added):
>
> **The generation of repetitive clocks can be modelled within the reduced model**, rather than requiring data from the data file 28. The list of signals 18 produced by step 16 is then used at step 20 to generate models that can serve to replay the recorded input signals within the POC file 10 in response to data drawn from the POC file 10.
>
> Page 9, lines 6-10:
>
> Figure 5 illustrates some example rules associated with output signals. A read enable signal is a strobe signal used to control reading from a data bus. **Correct operation of this signal is defined in a rule as a rising edge occurring within a time window 36 and then being maintained within that window.** The example illustrated shows this desired behaviour and would pass the rule.

From these and other portions of the specification, it appears that at least one embodiment of the invention involves a clock signal, otherwise known as "a periodic sampling reference". As a result, the claim limitation of using a reduced model to replay signals "without a periodic sampling reference" appears to be not tied to the disclosed

invention. As a result, the Examiner selected and applied prior art in the context of that which was disclosed, i.e. replaying the signals of the reduced model with a periodic sampling reference or clock signal. As the disclosure of the application fails to provide support for the phrase "without a periodic sampling reference" as argued by Applicant, the Examiner finds these arguments unpersuasive. These rejections are maintained.

4. Regarding new claim 35, Applicant offers to distinguish the limitations of claim 35 from the prior art of record with the following:

> The Examiner has suggested that Gupte at column 8, line 44 to column 9, line 8 teaches the subject matter of Applicants' claim 4. However, the cited portion of Gupte discloses that an input/output specification file comprises strobes and provides a particular example of a strobe signal that instructs the simulators to extract output vectors every 20 nanoseconds on particular output signals starting at 19 nanoseconds into the cycle. Thus, this passage of Gupte discloses discrete sampling of an output signal whose timing is controlled by a strobe signal. This has nothing to do with providing an output signal window within which a change in the output signal should occur to be indicative of correct operation.

The Examiner respectfully traverses this argument as follows:

The cited portion of Gupte clearly defines a window during which any given output vector is captured. The first vectors are allowed to occur at any time between 0 and 19 nanoseconds, when the first vector is captured. The second vectors are allowed to occur at any time between 19 and 29 nanoseconds, when the second vector is captured. This interpretation would have been obvious to a person of ordinary skill in the art. As has been explained above, Gupte clearly uses the captured "golden" vectors to ascertain correct operation during the standalone simulation. The cited portion and other portions of Gupte anticipate the limitations of Applicants' claim 4. Applicants' arguments in this regard are unpersuasive.

Response to Rejections under 35 U.S.C. § 103

Regarding the rejection of claims 6-11 and 22-27 under 35 U.S.C. § 103 as unpatentable over Gupte, Applicant argues primarily that:

> Inasmuch as Gupte does not teach the invention of independent claims 1 and 19 and because Applicants' claims recite "without requiring a periodic sampling reference for said output signal," Gupte actually teaches away from Applicants' claimed combination of elements and method steps.

The Examiner respectfully traverses this argument as follows:

The issue of the language "without requiring a periodic sampling reference" has been addressed above. The Examiner has traversed the argument that Gupte does not anticipate Applicants' claimed inventions above.

Regarding the rejection of claims 15 and 31 under 35 U.S.C. § 103 as unpatentable over Gupte and further in view of US Patent No. 5,544,067 to Rostoker, Applicant argues primarily that:

> Moreover, the Examiner's admission and recognition that Gupte "does not teach monitoring output signals other than at sampling points for that output signal" is very much appreciated. This admission clearly confirms Applicants' analysis of the independent claims and the fact that the claim language "without requiring a periodic sampling reference" clearly distinguishes over the Gupte reference.

The Examiner respectfully traverses this argument as follows:

The issue of the language "without requiring a periodic sampling reference" has been addressed above. The step of using including the language "without requiring a periodic sampling reference" in the independent claims refers to a step of "using at least a representation of said recorded input signals to form a reduced model to replay said recorded input signals to said subsystem model without requiring a periodic sampling reference". There does not appear to be any connection between the step of using in

the independent claims and "monitoring output signals other than at sampling points for the output signal". As the Examiner understands Applicants' claimed invention, monitoring is done to record the output signals, whereas the step of using in the independent claims is used to replay the recorded output signals.

Applicants' arguments linking the limitations of claims 15 and 31 to the steps of using in the independent claims are unpersuasive.

Outstanding Objections and Rejections

Specification

5. The use of the trademarks Verilog® and others has been noted in this application. They should be capitalized wherever they appear and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

Claim Rejections - 35 USC § 101

35 U.S.C. § 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

6. Claims 18, 33, 34, 42, and 43 rejected under 35 U.S.C. § 101 because the claimed invention is directed to non-statutory subject matter.

7. Regarding claim 18, the limitations recite a computer program *per se*, and are therefore nonstatutory. See MPEP § 2106(IV)(B)(1).

8. Regarding claims 33 and 42, the limitations recite a computer program *per se*, and are therefore nonstatutory. See MPEP § 2106(IV)(B)(1).

9. Regarding claims 34 and 43, the limitations recite a data abstraction not claimed as embodied in computer-readable media and is descriptive material *per se*. As a result, the claim is nonstatutory. See MPEP § 2106(IV)(B)(1).

10. To expedite a complete examination of the instant application the claims rejected under 35 U.S.C. § 101 (nonstatutory) above are further rejected as set forth below in anticipation of applicant amending these claims to place them within the four statutory categories of invention.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. § 112:

> **The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.**

11. Claims 1-43 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There are numerous problems with the specification, exemplified by the quotations provided below:

Page 12, lines 1-5 (emphasis added):

> This document is intended as a design specification for a software tool to be used by ARM, initially in the SoC group. In addition to specifying the product, it explains the benefits of the tool. **This document** specifies the requirements, but **does not attempt to fully document the detail of the implementation**.

Page 16, lines 9-14 (emphasis added):

> Since this tool provides a portable method of delivering an obfuscated verification suite & a means of improving the throughput of regression testing, it will have value to anyone who designs or uses IP blocks: SoC's, ASICs ASSPs, peripherals. Since the tool only eases part of the design process, rather than being particularly key to the process of SoC design, **this is a tool which ARM could market as a CAE product to the IP community.**

Page 19, lines 8-12 (emphasis added):

> **This could be implemented by detecting the time at which a signal changes and comparing this with the expected time.** Since there will typically be only a few different sets of setup and hold conditions for pins in a particular SoC or IP block, TBGen will allow the user to define timing specifications, and later associate these with particular pins.

Page 20, lines 10-15:

> A combination of source file and test vector file will be needed. The method of reading in test vectors should consider the efficiency of file access speed. TBGen should support a feature whereby signals which are busses or which share the same strobe requirement can be grouped together to keep the TBGen output file compact. Any other ideas to minimize the file size will be considered!

These sections of the specification speak to the nature of the disclosure as a suggestion of *what could be made* to form a "tool which ARM could market" rather than a concrete teaching of *how to make* the disclosed invention.

12. Specifically regarding the step of using, including the limitation "without requiring a periodic sampling reference", as found in claims 1, 17, 19, 32, 35, 40, and 41, the specification teaches:

Page 7, lines 5-9:

Figure 2 illustrates the full subsystem circuit model 2 and full surrounding circuits model 4, 6, 8 previously discussed in relation to Figure 1 but in this case shows the recording of a print on change (POC) file and message log 10. The mechanisms for recording such POC files and associated message logs are known and already provided within circuit simulation systems.

Page 7, line 24 – page 8, line 6 (emphasis added)

The generation of **repetitive clocks can be modeled within the reduced model**, rather than requiring data from the data file 28. The list of signals 18 produced by step 16 is then used at step 20 to generate models that can serve to replay the recorded input signals within the POC file 10 in response to data drawn from the POC file 10. Furthermore, **rules may be established** to associate the signals controlling whether a bidirectional signal is an input or an output with that bidirectional signal as well as **to define the times at which output signals should be sampled or the ranges of times within which output signals should change. For certain output signals, correct operation may be verified by observing that they have adopted a predetermined state (e.g. high, low, high impedance or changed) within a predetermined time window.** Within this class of output signals, some will also be strobe signals that themselves may be used to qualify correct operation of other output signals.

Page 9, lines 10-19:

The reduced model does not model the full behavior of the surrounding circuits and is quite insensitive to their internal workings, rather it concentrates on modeling the interaction between those surrounding circuits and the subsystem circuit model under test. This considerably reduces the simulation processing load and avoids the need to release proprietary information that may be contained within the full surrounding circuit models.

The disclosure of the instant application fails to describe "replay[ing] said recorded input signals to said subsystem circuit model without requiring a periodic sampling reference". A simulation of a circuit that is concerned with producing simulated response at the correct time is known in the art as a circuit timing simulation and pertains to the technology of circuit design timing analysis. A person of ordinary skill in the art would understand the timing of circuit responses as critical to properly "modeling the interaction between those surrounding circuits and the subsystem circuit model under test", as the timing of a circuit is widely recognized as a critical feature of a circuit's performance. Additionally, while the design by which a particular circuit is constructed could be regarded as proprietary information, the actual performance rating

of a circuit is widely available performance data critical to the successful marketing of the circuit. Timing data is not regarded as information that would be withheld during a combined simulation. Indeed there is more evidence in the specification that replaying the recorded signals *requires* a periodic sampling reference than to the contrary.

From the above and other teachings of the specification, the claimed step of using, including the limitation "without requiring a periodic sampling reference", as found in claims 1, 17, 19, 32, 35, 40, and 41 is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

13. This rejection is exemplary of the nature of the disclosure, which provides numerous proposed for features of the TBGen tool, but "does not attempt to fully document the detail of the implementation." While this admission is not a failure to comply with 35 U.S.C. § 112 *per se*, the disclosure is indeed deficient in regard to at least several claimed limitations. It would be apparent to a person of ordinary skill in the art that this disclosure is a proposal to create the claimed invention, not adequate written disclosure of an invention that the inventor(s), at the time the application was filed, had possession of the claimed invention.

14. Claims 1-43 are rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to

which it pertains, or with which it is most nearly connected, to make and/or use the invention.

There are numerous problems with the specification, exemplified by the quotations provided below:

Page 13, lines 12-26:

> A tool is proposed which takes the output from a simulation using a potentially complex test bench incorporating VHDL/Verilog models, Denali models, Specman models, and from this generates a "minimal test bench". This minimal test bench then allows the simulation to be replayed exactly whilst preserving exact timing but without the need for the original test bench. This tool, which we are naming "TBGen" (Test Bench Generator), provides a test bench delivery mechanism which encapsulates test bench IP. It offers three key advantages!
> - removes the need for licenses to the test bench IP, eg Specman/Denali,
> - obfuscates the test bench IP,
> - significant improvement in simulation speed.

This teaching establishes that "TBGen" broadly refers to the disclosed invention. The disclosure is not enabling for allowing "the simulation to be replayed exactly whilst preserving exact timing", especially where claims 1, 17, 19, 32, 35, 40, and 41 recite a step of replaying recorded input signals "without requiring a periodic sampling reference". Clock signals, which are functionally equivalent to "a periodic sampling reference", are well known in the art. A person of ordinary skill in the art would be unable to make and use a simulation that replays recorded input signals "without requiring a periodic sampling reference".

Page 15, lines 4-12 (emphasis in original):

> Even if the original test bench relies on licensable IP and 3rd party products, a particular simulation run can be reconstructed without needing to deliver any test bench IP. The only restriction that this imposes is that it is impractical to modify the test stimuli. However, note: *it is still possible to attach protocol checkers and view the progress of the simulation*. This might be seen as a restriction on the functionality of this tool, but in practice a customer who wishes to make significant modifications to a test bench is likely to have suitable tools and models to

> achieve verification of their design which incorporates ARM IP. The TBGen test bench delivers an "out of box" test to the end user.

The term "ARM IP" appears to be in reference to the assignee of the instant application. This presents considerable challenges to a person of ordinary skill in the art attempting to make and use the claimed invention, because "ARM IP" may not be well known, available, or desirable. A person of ordinary skill in the art would be unable to make and use an invention that uses the step of using as exemplified in claim 1 based on these teachings regarding ARM IP.

> Page 20, lines 10-15:
>
> A combination of source file and test vector file will be needed. The method of reading in test vectors should consider the efficiency of file access speed. TBGen should support a feature whereby signals which are busses or which share the same strobe requirement can be grouped together to keep the TBGen output file compact. Any other ideas to minimize the file size will be considered!

This portion of the specification suggests that the claimed invention should solve particular problems but does not offer solutions. The disclosure offers no direction on the solution to these problems. A person of ordinary skill in the art would be left entirely to his own skills of invention in order to follow these teachings. A person of ordinary skill in the art would be unable to make and use an invention that uses the steps of recording and using as exemplified in claim 1.

15. Specifically regarding the phrase "without requiring a periodic reference signal" as recited in all pending independent claims 1, 17, 19, 32, 35, 40, and 41, the disclosure is not enabling for this feature. As noted above, several sections of the disclosure appear to at least suggest the requirement of a clock or periodic reference signal.

Page 4, lines 15-22 (emphasis added):

The configuration files used in conjunction with the recorded signals could take various different forms, but are preferably files specifying whether signals are input signals, output signals or bidirectional signals. This data may then be used to control the automatic generation of the required portion of the reduced model **to replay input signals in the correct sequence and time**, or capture output signals with appropriate timing constraints and interdependencies associated therewith. This also allows timing models to be defined for association with signals thereby reducing the overall work required to produce a model.

Page 4, line 30 – page 5, line 5 (emphasis added):

Some of the output signals may be strobe signals that control the sampling of other output signals and this behaviour can be modelled within the reduced model. Both the strobe output signal and the strobed output signal may have time windows associated with them. A strobe output signal should change to its desired predetermined state (e.g. strobe signals may only be active on a rising edge and otherwise ignored) within an associated strobe output signal time window and the strobed output signals should hold their value within a strobed signal time window. The strobed signal time window may be asymmetrically disposed about is sampling point and may be surrounded by a settling window and a settled window. More than one signal may strobe a strobed signal.

Page 7, lines 13-17 (emphasis added):

The generation of repetitive clocks can be modelled within the reduced model, rather than requiring data from the data file 28. The list of signals 18 produced by step 16 is then used at step 20 to generate models that can serve to replay the recorded input signals within the POC file 10 in response to data drawn from the POC file 10.

Page 9, lines 6-10:

Figure 5 illustrates some example rules associated with output signals. A read enable signal is a strobe signal used to control reading from a data bus. **Correct operation of this signal is defined in a rule as a rising edge occurring within a time window 36 and then being maintained within that window.** The example illustrated shows this desired behaviour and would pass the rule.

MPEP 2164.01(a) provides eight factors to consider when determining undue experimentation:

These factors include, but are not limited to:
(A) The breadth of the claims;
(B) The nature of the invention;
(C) The state of the prior art;
(D) The level of one of ordinary skill;
(E) The level of predictability in the art;
(F) The amount of direction provided by the inventor;
(G) The existence of working examples; and
(H) The quantity of experimentation needed to make or use the invention based on the content of the disclosure.

In considering these factors, the Examiner respectfully submits:

(A) The phrase under discussion, "without requiring a periodic reference signal", is a negative limitation which has breadth covering all implementations *except* those with a "periodic reference signal". While not improper *per se*, this negative limitation is nevertheless extremely broad.

(B) This invention relates to the design and simulation of complex integrated circuits and is therefore an invention legitimately classified as high technology.

(C) The state of the prior art, as admitted in the background of the specification as well as made of record, achieves the claimed step of using with a clock signal, otherwise referred to as "a periodic reference signal". A search of the prior art does not reveal methods of performing circuit timing analysis without the use of such.

(F) The state of the disclosure has been addressed above. An examination of the specification as filed fails to provide support for this phrase except in claim 1 and where the text of claim 1 appears in the specification. Mere recitation of this phrase does not provide adequate enablement and the disclosure provides, at best, conflicting direction.

(G) The Examiner would appreciate evidence of existence of working examples. As addressed above regarding the state of the prior art, circuit timing simulations that do not require a periodic reference signal are at least not widely known.

(H) The criticality of highly precise timing measurements in circuit timing analysis, often representing events on the scale of nanoseconds, cannot be understated. The disclosure provides neither explicit nor implicit nexus between

replaying the recorded signals in correct sequence and time (page 4, lines 15-22) and the claimed step of using "without requiring a periodic sampling reference". The quantity of experimentation needed to make or use the invention therefore covers the entire process of discovery and or invention of the methods by which Applicants' invention achieves the claimed step of using.

In general, the disclosure fails to enable and provides inadequate written description for claimed limitations too numerous to completely identify. In remedying these situations under 35 U.S.C. § 112, first paragraph, Applicant is respectfully reminded of the provisions of 35 U.S.C. § 132(a) that states that no amendment shall introduce new matter into the disclosure of the invention, however new material can be added under 37 CFR 1.53 as, for example, a continuation-in-part.

The Examiner has made this action non-final to allow Applicant an opportunity to respond to the new grounds of rejection under 35 U.S.C. § 112, first and second paragraphs. The Examiner apologizes for not raising these issues in the previous office action.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

16. Claims 1-43 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

17. Independent claims 1, 17, 19, 32, 35, 40, and 41 all recite the phrase "without requiring a periodic sampling reference". It is unclear what this limitation represents. It is unknown how to make the determination that a periodic sampling reference is *required*. This is a relative term that may or may not be indicative of the performance of the system. For example, some inventions of prior art could provide some functionality without a periodic sampling reference, however they might perform very badly. Therefore the question is raised whether the periodic sampling reference is truly *required* in the prior art.

18. It is further unclear what the metes and bounds of this limitation are. In restricting the claimed invention to performing "without requiring a periodic sampling reference", it is unknown whether the same invention operates without requiring a clock signal, an acyclic reference signal, an isosynchronous reference signal, an asynchronous reference signal, an erodonic reference signal, an iterative electromagnetic pulse, a rising voltage at regular intervals, or some other concept that is not narrowly defined as "a periodic sampling reference".

19. Regarding claims 34 and 43, it is unclear what is meant by "a reduced hardware model synthesised from said reduced model". It is unclear how a "reduced hardware model" differs from the reduced model of claim 1 which is a model of one or more

surrounding circuits. Presumably the reduced model of claim 1, being a reduced model of hardware, constitutes a "reduced hardware model". It is unclear whether a "reduced hardware model" is tangible or rather nonfunctional descriptive material. It is unclear what constitutes "synthesising" a reduced hardware model from a reduced model.

Claim Interpretation

In the interest of compact prosecution, examiner makes the following claim interpretations in order to apply prior art to the claims. See *Ex parte Ionescu*, 222 USPQ 537 (Bd. Pat. App. & Inter. 1984).

20. Independent claims 1, 17, 19, 32, 35, 40, and 41 are interpreted wherein the phrase "without requiring a periodic sampling reference" does not preclude the use of a clock signal or similar.

21. Claims 34 and 43 cannot be interpreted without relying on significant speculation and therefore the Examiner does not believe it would be productive to apply art until the issues under 35 U.S.C. § 112, second paragraph are resolved.

22. Applicants' arguments regarding the prior art have been considered and were found unpersuasive as a result of a lack of support in the disclosure. Providing adequate support in the disclosure for those arguments could influence the Examiner's opinion of those arguments regarding the prior art.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

23. Claims 1-5, 12-14, 16-21, 28-30, 32-33, 35-37, and 41-42 are rejected under 35 U.S.C. § 102(b) as being anticipated by Gupte et al., US Patent No. 5, 903, 475.

Regarding claim 1, Gupte et al. teaches a method for simulating circuits wherein the simulation performs a test sequence of data processing operations (column 2, lines 23-33),

including simulation operation of both a subsystem under test and one or more surrounding circuits (column 2, lines 7-22; column 9, lines 22-34) where a system simulation is equivalent to testing a subsystem under test in conjunction with the surrounding components that comprise the system,

recording input signals to and output signals from said subsystem circuit while performing said test sequence of data processing operations (column 2, lines 7-22; column 6, lines 53-64; column 9, lines 18-21),

using a representation of recorded input signals to form a reduced model to compare output signals with one or more predetermined characteristics indicative of correct operation (column 2, lines 7-22; column 6, lines 41-52),

whereby a subsystem under test and reduced model may be used to simulate the subsystem under test performing the test sequence of data processing operations

without simulating operation of one or more surrounding circuits (column 2, lines 7-22; column 6, lines 41-64).

Regarding claim 2, Gupte et al. teaches the use of a configuration file including data specifying input signals, output signals, and bi-directional signals exchanged with the subsystem circuit in order to form the reduced model (column 8, line 44 – column 9, line 8)

Regarding claim 3, Gupte et al. teaches that signals from the subsystem are used to determine when bi-directional signals can be driven making allowance for variations in delays inherent in output loads (column 10, lines 11-17).

Regarding claim 4, Gupte et al. teaches that the reduced model includes a rule having an output signal time window within which a change in said output signal to a predetermined output signal value should occur to be indicative of correct operation (column 8, line 44 – column 9, line 8).

Regarding claim 5, Gupte et al. teaches recording output signals from a subsystem circuit under test (column 8, line 44 – column 9, line 8). While Gupte et al. does not explicitly disclose that the output signals values are one of: high; low; changed; and high impedance, it is inherent that signals in a digital circuit are referred to by the values in the enumerated group or by equivalent terms. Therefore, by recording output

signals, the invention of Gupte et al. records values which are one of: high; low; changed; and high impedance.

Regarding claim 12, Gupte et al. teaches that the full subsystem circuit model from which said input signals and said output signals are recorded may be different from that to which said input signals are subsequently replayed and from which output signals are subsequently analysed (column 2, lines 7-22; column 9, lines 22-34).

Regarding claim 13, Gupte et al. teaches that the full subsystem circuit model may change between different versions during regression testing (column 17, lines 14-25; column 18, lines 19-24).

Regarding claim 14, Gupte et al. teaches that the full subsystem circuit may change between being one of an RTL model, a netlist model, or other software views (column 9, lines 42-46; column 7, lines 36-40; column 7, lines 55-62; column 8, lines 6-17).

Regarding claim 16, Gupte et al. teaches recording progress messages for replay during regression testing (column 9, line 58 – column 10, line 4). Statistics are presumed equivalent to progress messages.

Regarding claim 17, the limitations recite an apparatus which performs the method as recited by claim 1. As the invention of Gupte et al. is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 17 are rejected by reasoning similar to that used to reject the limitations of claim 1 above.

Regarding claim 18, the limitations recite a computer program product comprising a computer program for controlling a computer to perform a method as recited in claim 1. As the invention of Gupte et al. is embodied in a computer (Fig. 2; column 4, lines 5-7), the limitations of claim 18 are rejected by reasoning similar to that used to reject the limitations claim 1 above.

Regarding claims 19, 20-21, and 28-30, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claims 4-5 and 12-14. As the invention of Gupte et al. models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 19, 20-21, and 28-30 are rejected by reasoning similar to that used to reject claims 1, 4-5, and 12-14 above.

Regarding claim 32, the limitations recite an apparatus for modeling a data processing apparatus corresponding to the apparatus for creating a model of a data processing apparatus as recited in claim 17. As the invention of Gupte et al. is

embodied in a computer (Fig. 2; column 4, lines 5-7) and performs a simulation of the data processing apparatus (column 1, lines 62-65; column 2, lines 7-22) the limitations of claim 32 are rejected by reasoning similar to that used to reject the limitations of claim 17 above.

Regarding claim 33, the limitations recite a computer program product comprising a computer program controlling a computer to perform a method as claimed in claim 19. As the invention of Gupte et al. is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 33 are rejected by reasoning similar to that used to reject the limitations of claim 19 above.

Claim 35 recites a combination of limitations found in claims 1 and 4 and is rejected for the same reasons given above for claims 1 and 4.

Claims 36 and 37 recite combinations of limitations found in claims 5 and 3, respectively, and are rejected for the same reasons given above for claims 5 and 3.

Claim 41 recites an apparatus that performs the method of claim 1. As the invention of Gupte et al. is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 43 are rejected by reasoning similar to that used to reject the limitations of claims 1 and 4 above.

Claim 42 recites a computer program product that performs the method of claim 35. As the invention of Gupte et al. is embodied in a computer (Fig. 2; column 4, lines 5-7) the limitations of claim 42 are rejected by reasoning similar to that used to reject the limitations of claims 1 and 4 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claims 6-11, 22-27, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gupte et al. as applied to claims 1 and 19 above.

Regarding claim 6, Gupte et al. does not teach using a strobe signal in the model to trigger sampling of a strobed output signal and verify the strobed output signal. However, Gupte et al. does disclose a strobe rule which samples selected signals at regular intervals and to compare the sampled values with known good values to verify that the output signal is correct (column 8, line 44 – column 9, line 8). The strobe rule of Gupte et al. provides the same functionality as the limitations recited in claim 6. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to modify the strobe rule of Gupte et al. to sample strobed output signals in

response to a strobe signal in the model to simplify creating of the reduced model or to better facilitate the design of circuits which always involve strobe signals. Such a modification would preclude the generation of faulty reduced models that fail to properly sample the strobed signals. The combination could be achieved by a rule that defines the relationship between a strobe signal and one or more strobed signals, and the tolerances related to the strobe signal and sampling the strobed signals.

Regarding claim 7, Gupte et al. does not teach a rule that includes a strobe output signal time window. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would be obvious to a person of ordinary skill in the art at the time of applicant's invention to define a time window within which a change in strobe output signal to match a predetermined strobe output signal value should occur as a tolerance related to the strobe signals.

Regarding claim 8, Gupte et al. does not teach a rule that includes a strobed output signal time window within which said strobed output signal should hold a predetermined strobed output signal value to be indicative of correct operation. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a time window within which a strobed output signal should hold a predetermined

strobed output signal value to indicate correct operation as a tolerance related to sampling the strobed signals.

Regarding claim 9, Gupte et al. does not teach a strobed output signal time window that is non-symmetrically disposed about a time when said strobed output signal is sampled. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a time window that is non-symmetrically disposed about a time when said strobed output signal is sampled as a tolerance related to sampling the strobed signals.

Regarding claim 10, Gupte et al. does not teach a settling time window that is at least partially surrounded by a settling time window within which said strobed output signal is permitted to change. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a settling time window that is at least partially surrounded by a settling time window as a tolerance related to sampling the strobed signals.

Regarding claim 11, Gupte et al. does not teach a settling time window that is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change. However, the combination made in the rejection of claim 6 above includes tolerances related to a strobe signal and sampling one or more strobed signals. It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to define a settling time window that is at least partially surrounded by a settled time window within which said strobed output signal is not permitted to change as a tolerance related to sampling the strobed signals.

Regarding claims 22-27, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claims 6-11. As the invention of Gupte et al. models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 22-27 are rejected by reasoning similar to that used to reject claims 6-11 above.

Claim 38 recites a combination of limitations found in claims 1, 4, and 6 and are rejected for the same reasons given above for claims 1, 4, and 6. Gupte anticipates the limitations of claims 1 and 4 and renders obvious the limitations of claim 6. A recombination of those limitations would be similarly obvious in view of Gupte.

25. Claims 15, 31, and 39 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Gupte et al. as applied to claims 1 and 19 above, and further in view of Rostoker et al. US Patent No. 5,544,067.

Regarding claim 15, Gupte et al. does not teach monitoring output signals other than at sampling points for that output signal. Rostoker et al. teaches monitoring output signals within the circuit diagrams (Fig. 19, references 1910, 1912, 1914, and 1916; column 11, lines 65-67; column 30, lines 47-60). It would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to combine monitoring output signals within the circuit diagrams as in the invention of Rostoker et al. with the system simulation of Gupte et al. in order to better facilitate the designer's understanding of the internal operation of the subsystem circuit under test. The combination could be achieved by a rule which allows the designer to specify monitoring output signals within the subsystem circuit under test.

Regarding claim 31, the limitations recite a method for modeling a data processing apparatus corresponding to the method for creating a model of a data processing apparatus as recited by claim 1 and further limited by claim 15. As the invention of Gupte et al. models a data processing apparatus (column 1, lines 62-65; column 2, lines 7-22), the limitations of claims 31 are rejected by reasoning similar to that used to reject claim 15 above.

Claim 39 recites a combination of limitations found in claims 1, 4, and 15. Gupte anticipates the limitations of claims 1 and 4 and renders obvious the limitations of claim 15. A different combination of those limitations would be similarly obvious in view of Gupte.

Conclusion

New grounds of rejection have been entered in this action. Consequently, this action is NON-FINAL.

Art considered pertinent by the examiner but not applied has been cited on form PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Proctor whose telephone number is (571) 272-3713. The examiner can normally be reached on 8:30 am-4:30 pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin J Teska can be reached on (571) 272-3716. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-3713.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained

from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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